# USB PD and Other Fast Charging Protocol Chip CH238

Datasheet

Version: 1A

https://wch-ic.com

## 1. Overview

CH238 is a Type-C single-port fast charging protocol chip in QFN16 package, which supports Type-C fast charging protocols such as PD3.0/2.0, PPS, and other fast charging protocols such as BC1.2, etc. CH238 supports full-feedback current regulation mode and incremental open-loop current regulation mode, which can be used for direct opto-coupler-controlled voltage regulation or FB-flooding current-voltage regulation, and it is built-in NMOS with power path, with VBUS detection and discharging function, and provides over-temperature protection.

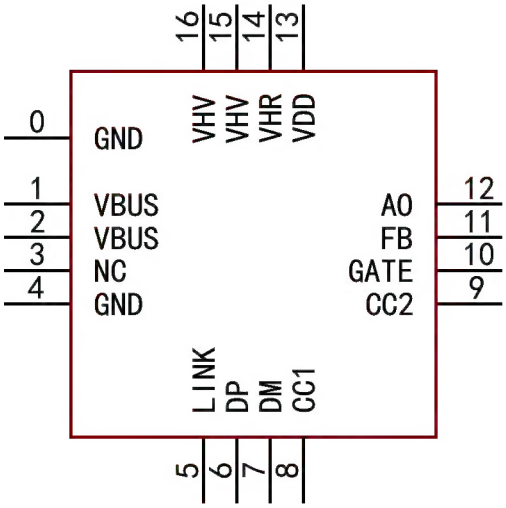
## 2. Features

- Support 3.3V-22V wide voltage inputs
- Built-in NMOS, 25V tolerant voltage and 3.25A maximum continuous on-state current.
- Support PD2.0/3.0, PPS, BC1.2 and other fast charging protocols
- Support full feedback current adjustment mode, which can be used for direct optocoupler control voltage regulation
- Support TL431 and DC-DC devices such as FB irrigation current and voltage regulation, voltage regulation accuracy of 20mV
- Built-in over-temperature protection OTP

## 3. Applications

- AC Power Adapter
- Car Charger
- UPS
- Mobile Power

# 4. Package




CH238P(QFN16)

# 5. Pins

| Pin No. CH238P | Pin Name | Pin Description |
|---|---|---|
| 15/16 | VHV | High voltage positive power supply input terminal, external power decoupling capacitor is required |
| 13 | VDD | Internal power regulator LDO output and internal working power input, external capacitor 1uF decoupling capacitor is required |
| 0,4 | GND | Common ground |
| 11 | FB | Adjustable sink current input for voltage feedback adjustment |
| 10 | GATE | Gate control terminal of external NMOS power tube |
| 12 | AO | Used for direct optocoupler control voltage regulation |
| 8 | CC1 | Type-C PD fast charging protocol communication bus |
| 9 | CC2 | |
| 6 | DP | Type-A fast charging protocol communication bus |
| 7 | DM | |
| 1,2 | VBUS | Power output pin, VBUS detection and discharge pin |
| 14 | VHR | Select the driving mode of power management:<br>If VHR is shorted to VDD, AO is valid, and is used for direct photocoupling control voltage regulation;<br>If VHR is suspended or grounded, AO is invalid, and is used for FB sink current voltage regulation. |
| 5 | LINK | Multi-chip communication pins |

| | | |
|---|---|---|
| 3 | NC | Reserved, unconnected |

# 6. Typical Application

Figure 6.1 Refer to schematic diagram of CH238 with FB adjustment

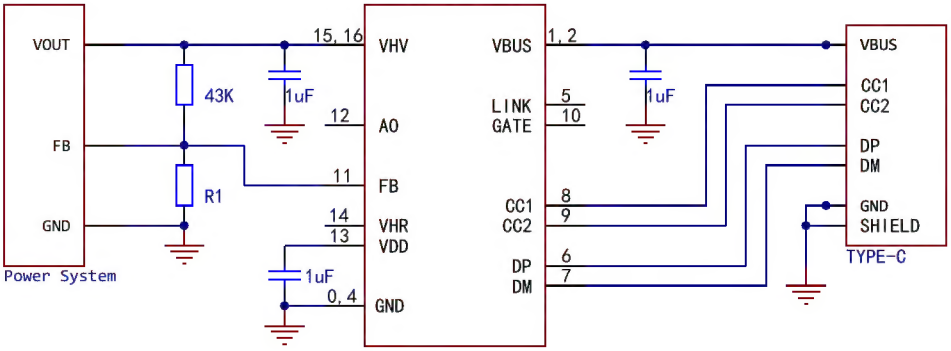
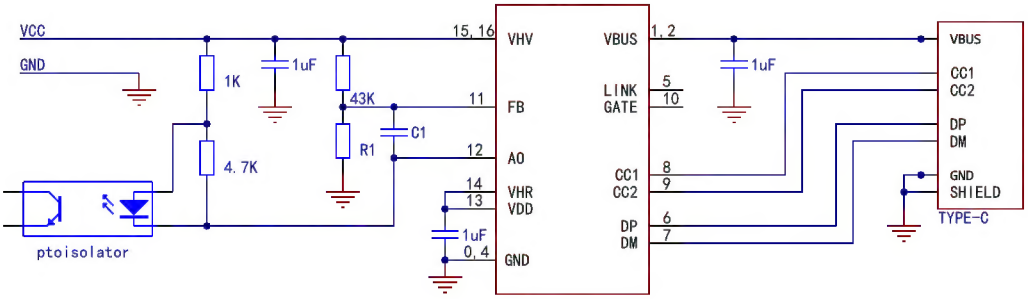



Figure 6.2 Reference schematic diagram of CH238 with optical coupler adjustment



# 7. Function Description

## 7.1 VHV/VDD Pin

The VHV pin of CH238 is the high-voltage power supply input pin of the chip. It is connected to the output end of the power supply. The 1uF decoupling capacitor needs to be connected to the external one. The chip is connected to the LDO and the high-voltage NMOS drain inside the chip. The VDD pin is the LDO output of the CH238 internal power regulator and the internal working power input. The 1uF decoupling capacitor needs to be connected to the external one.

## 7.2 Power Supply Path NMOS and Gate Driver

The CH238 has a built-in power supply path NMOS, which has a tolerant voltage of 25V and a maximum continuous conduction current of 3.25A, which can be used to control the conduction of the power supply from VHV to VBUS. The GATE pin of the chip is the lead-out pin of the internal gate driver, which is used to drive the internal NMOS, and can also drive the external N-MOSFET.

If a lower on-impedance is required, an external parallel N-MOSFET can be connected.

## 7.3 FB/AO/VHR Pin

CH238 supports full feedback current regulation mode, which can be used for direct optocoupler control voltage regulation, and also supports incremental open-loop current regulation mode, which can be used for FB sink current voltage regulation. The VHR pin can be used for driving mode selection. If VHR short-connects VDD, AO is valid, and if VHR is suspended or grounded, AO is invalid.

When CH238 is in full feedback current regulation mode, the AO pin can directly control the AC-DC power supply optocoupler, and the internal reference voltage of FB is about 1.2V. As shown in Figure 6.2, the upper bias resistor on the FB pin is fixed to 43K 1% or higher accuracy. The lower bias resistor R1 is selected according to the different default power voltage. R1 can be selected at 3.3V by default. The feedback capacitor C1 is used to adjust the speed of the lifting voltage, and the smaller the capacitance value, the faster the adjustment.

When CH238 is in incremental open-loop current regulation mode, there is a controllable sinking current inside the FB pin, and the FB pin of the DC-DC system can control the output voltage of the power supply system. When in use, set the upper bias resistor on the FB pin to be fixed to 43K 1% or higher accuracy, and calculate the lower bias resistor based on the FB voltage, so that the default output voltage of the power supply system is 3.3V.

Take the R1 resistance calculation in Figure 6.1 as an example:

For DC-DC system with FB voltage of 0.8V, the upper bias is 43K, the lower bias resistor R1 is 13.7K, and the default output voltage is:

$$((39/13.7)+1)*0.8 = 3.31V$$

## 7.4 CC1/CC2/DP/DM Pin

The CC1/CC2 pins are used for equipment access detection and PD protocol handshake, and the CH238 supports the current broadcast of DFP mode 500mA, 1.5A or 3A defined by the Type-C protocol.

The DP/DM pin is used to shake hands with related protocols such as BC1.2.

### 7.5 VBUS Pin

The VBUS pin is connected to the high-voltage NMOS source inside the chip, which is the output end of the VBUS power supply. At the same time, it provides overvoltage protection and power supply discharge functions, which can speed up the adjustment of power supply voltage and discharge the residual electricity of the Type-C interface.

# 8. Function Description

**8.1 Absolute Maximum Value** (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

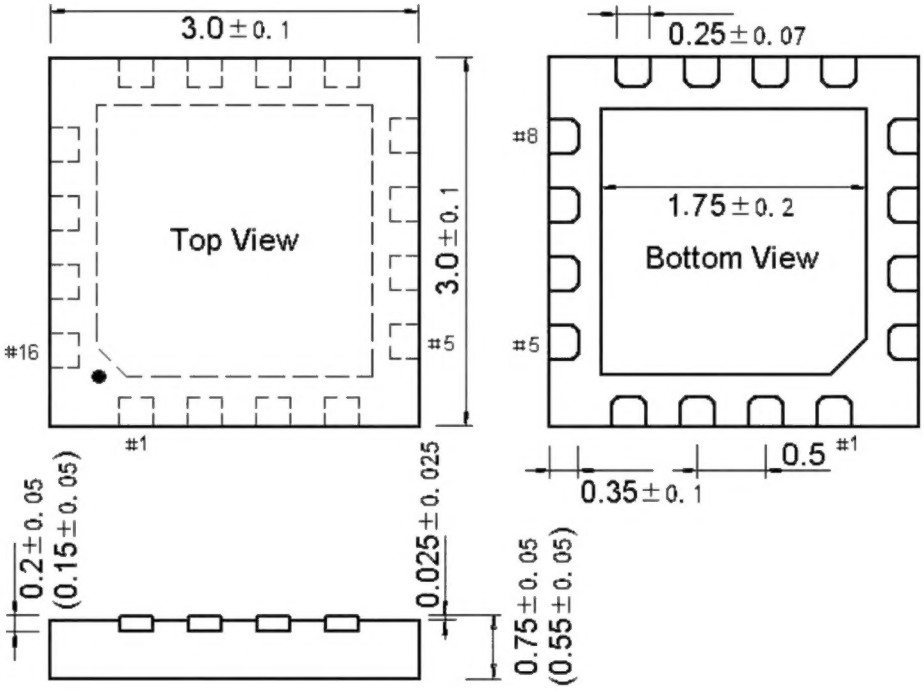
| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| TA | Ambient temperature during operation | VHV=4V~16V | -40 | 110 | ℃ |
| | | VHV=2.8V~22V | -40 | 85 | ℃ |
| TS | Ambient temperature during storage | | -55 | 125 | ℃ |
| VHV | Operating power supply voltage (VHV pin is connected to power supply, GND pin is grounded) | | -0.5 | 25.0 | V |
| VIO | Voltage on non-high voltage pins | | -0.5 | VDD+0.5 | V |
| VIOCC | Self-low-voltage, but can tolerant the voltage on high-voltage pins (CC1, CC2) | | -0.5 | 22.0 | V |
| VIOHV | Voltage on high voltage pin (VBUS, AO) | | -0.5 | 25.0 | V |
| VIOHX | Voltage on the self-boost high voltage pin (GATE) | | -0.5 | VHV+6.5 | V |
| INMOS | Continuous conduction current of NMOS power tube | | | 3.5 | A |
| PD | Maximum power consumption of the entire chip (VHV voltage * current + discharge power consumption) | | | 300 | mW |

**8.2 Electrical Parameters** (Test condition: TA = 25℃)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VHV | High voltage supply voltage VHV | | 3.3 | 5.2 | 22 | V |
| ICC | Power current during operation | VHV=20V | | 1.2 | 15 | mA |
| | | VHV=5V | | 1.0 | 8 | |
| VLDO | Internal VDD power regulator LDO output voltage | | 3.2 | 3.3 | 3.4 | V |
| RNMOS | On-resistance of NMOS power tube | | 14 | 20 | 30 | mΩ |
| ILDO | Internal VDD power regulator LDO external load capacity | | | | 10 | mA |
| IFB | Sink current on FB pin | | | 0~511 | | uA |
| ILINK | Pull-up current on LINK pin (to VDD) | | 20 | 40 | 80 | uA |
| IDIS | VBUS pin discharge current | | 5 | 10 | 16 | mA |
| TOTA | Reference threshold temperature of CH238 ultra-temperature alarm module OTA | | | 125±15 | | ℃ |
| VR | Power-on reset voltage threshold | | 2.5 | 2.7 | 2.9 | V |

# 9. Package Information

| Package Form | Body Size | Pin Pitch | | Order Model |
|---|---|---|---|---|
| QFN16 | 3*3mm | 0.50mm | 19.7mil | CH238P |

*Note: The dimensioning unit is mm.*

## 9.1 QFN16